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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,022	08/02/2001	Guy Harlan Humphrey	10010504-1	7798

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AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,022	HUMPHREY, GUY HARLAN	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7,12,14,15 and 18-21* is/are rejected.

7)☒ Claim(s) *2,5,6,13,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/24/04 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 7, 12, 14-15 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,747,854, issued to Gotou.

As per claim 3, Gotou discloses an output driver (Fig. 33) that drives an output signal onto an output pad (the pad at the intersection of the drains of FETs P2 and N2) of an integrated circuit (the Gotou's CMOS inverter is integrated in a semiconductor substrate, column 1, line 66, and column 9, lines 18-21 and lines 60-65 teaches independent FETs in parallel, the input and output pads must be provided in order for the CMOS inverter to be used), comprising:

a first switchably conductive device (N1) characterized by a first threshold voltage (column 19, table 1, N1=0.5 volts) of a given polarity (the positive voltage which starts to turn ON N1), coupled between the output pad (the intersection of the drains of P2 and N2) and a voltage source (5V and GND), a control input (gate of N1) receives a driving signal (at the gate) to turn ON (when the driving voltage is greater than or equal to the first threshold voltage) or to turn OFF (when the driving voltage is less than the first threshold voltage); and

a second switchably conductive device (N2) independent from the first switchably conductive device (N1) (the driving signal independently controls the gates of N1 and N2) characterized by a second threshold voltage (column 19, table 1, N2=1 volts) of the given polarity (thresholds of both N1 and N2 are positive) which is greater than the first threshold voltage (compare 1 volts and 0.5 volts), coupled between the output pad (the intersection as shown) and the voltage source (5V and GND), a control input (gate of N2) receives the driving signal (at the gate) to turn ON (when the driving voltage is greater than or equal the second threshold voltage) or to turn OFF (when the driving voltage is less than the second threshold voltage);

wherein the first switchably conductive device and the second switchably conductive device together operate to reduce the slew rate of the transition edges driven onto the output pad of the integrated circuit (the recited function is merely the result of operation of the output driver having the recited structure when the input node receives an input signal).

As per claim 4, the recited first and second FETs read on FETs N1 and N2, respectively.

As per claim 1, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Gotou teaches the circuit, he inherently teaches the method.

As per claim 7, this claim is rejected for the same reasons noted in claim 1.

As per claim 14, Gotou discloses an output driver (Fig. 33) that drives an output signal onto an output pad (the intersection of the drains of P2 and N2 or P1 and N1) of an integrated circuit, comprising:

a first switchably conductive device (P1) characterized by a first threshold voltage (column 19, table 1, P1=-0.5 volts) of a given polarity (the negative voltage which starts to turn ON P1), connected between the output pad (the intersection as shown) and a voltage source (5V and GND), a control input (gate of P1) receives a driving signal (at the gate) to turn ON (when the driving voltage is less than or equal to the first threshold voltage) or to turn OFF (when the driving voltage is greater than the first threshold voltage); and

a second switchably conductive device (P2) independent from the first switchably conductive device (P1) (the driving signal independently controls the gates of P1 and P2) characterized by a second threshold voltage (column 19, table 1, P2=-1 volts) of the given polarity (thresholds of both P1 and P2 are negative) which is less than the first threshold voltage (compare -1 volts and -0.5 volts), connected between the output pad (the intersection as shown) and the voltage source (5V and GND), a control input (gate of P2) receives the driving signal (at the gate) to turn ON (when the driving voltage is less than or equal to the second threshold voltage) or to turn OFF (when the driving voltage is greater than the second threshold voltage);

wherein the first switchably conductive device and the second switchably conductive device together operate to reduce the slew rate of the transition edges driven onto the output pad of the integrated circuit (the recited function is merely the result of operation of the output driver having the recited structure when the input node receives an input signal).

As per claim 15, the recited first and second FETs read on FETs P1 and P2, respectively.

As per claim 12, this claim is merely a method to operate an apparatus having the structure discussed in claim 14 above, since Gotou teaches the circuit, he inherently teaches the method.

As per claim 18, this claim is rejected for the same reasons noted in claim 12.

As per claims 19-21, these claims are rejected for the same reasons noted in claims 3, 1 and 7, respectively.

Response to Arguments

3. Applicant's arguments filed 7/24/04 have been fully considered but they are not persuasive.

Regarding the argument Gotou does not teach an output driver that drives an output signal onto an output pad of an integrated circuit, but rather, Gotou teaches a CMOS inverter (Figs. 9A, 9B), remarks section, page 16.

A reference, US Patent No. 6,515,528, has been cited to show that an inverter circuit (Fig. 1, section 4) is used as an output driver circuit, i.e., see the abstract. The examiner further notes the fact that Gotou names the circuit shown in Fig. 33 is a CMOS inverter whereas the claimed circuit is an output driver does not distinguish the claimed circuit from the Gotou circuit because the Gotou's inverter circuit has the structure recited in the claim. The output pad is the pad at the connection of drains of N2 and P2 because this is the point where an inverted signal of the input signal is outputted. The Gotou's CMOS inverter is integrated in a semiconductor substrate, the input and output pads must be provided in order for the CMOS inverter to be used.

It is clear that when a digital signal is applied to the input of the inverter shown in Fig. 33, the inverter will drive an output signal which is the inverted signal of the input signal onto the output pad.

Regarding the argument Gotou teaches MOS transistors are for used in a logic gate for reducing through current during the state transitions and reducing the power consumption whereas the circuit of the current invention is used in output driver to pull an output pad of an integrated circuit high or low, remarks section, page 17.

The examiner noted the fact that Gotou teaches CMOS inverter for used in a logic gate for reducing through current during the state transitions and reducing the power consumption. However, the Gotou's inverter also performs the function to pull an output pad of an integrated circuit high or low. A CMOS inverter functioned as an output driver is discussed in the preceding response, i.e., US Patent No. 6,515,528. Pulling an output pad (connected to the output of the CMOS inverter) of an integrated circuit high or low is clearly the operation of the inverter. The drawings shown in Figs. 3A and 3B of the present invention are clearly the waveforms of the IN/OUT signals of an inverter.

Regarding the argument the logic gates shown in Gotou, including a CMOS inverter, a NAND gate and a NOR gate are not standard components used as pull-up or pull down devices in an output driver, Remark Section, page 18.

Please see the cited prior art, i.e., US Patent No. 6,515,528.

Allowable Subject Matter

4. Claims 2, 5-6, 13 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-6 are allowable because the prior art of record fails to disclose or suggest the inclusion of one or more switchably conductive devices each having different threshold voltage for reducing the slew rate of the output signal as recited in claim 5. The inclusion of one or more switchably conductive devices each having different threshold voltage defines patentability over the prior art of record because Gotou teaches an output driver for reducing through current during the state transitions and reducing the power consumption which need to use only two switchably conductive devices, therefore, there is no motivation by a person skilled in the art to add more switchably conductive devices in parallel to the first and second switchably conductive devices.

Claims 2, 13 and 16-17 are allowable for the same reasons noted in claim 5.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/1/04

Minh Nguyen
Primary Examiner
Art Unit 2816